



TFT LCD Preliminary Specification

MODEL NO.: N170C2 - L02

Customer : _____

Approved by : _____

Note :

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval
	



- CONTENTS -

REVISION HISTORY	3
1. GENERAL DESCRIPTION	4
1.1 OVERVIEW	
1.2 FEATURES	
1.3 APPLICATION	
1.4 GENERAL SPECIFICATIONS	
1.5 MECHANICAL SPECIFICATIONS	
2. ABSOLUTE MAXIMUM RATINGS	5
2.1 ABSOLUTE RATINGS OF ENVIRONMENT	
2.2 ELECTRICAL ABSOLUTE RATINGS	
2.2.1 TFT LCD MODULE	
2.2.2 BACKLIGHT UNIT	
3. ELECTRICAL CHARACTERISTICS	6
3.1 TFT LCD MODULE	
3.2 BACKLIGHT UNIT	
4. BLOCK DIAGRAM	10
4.1 TFT LCD MODULE	
4.2 BACKLIGHT UNIT	
5. INPUT TERMINAL PIN ASSIGNMENT	11
5.1 TFT LCD MODULE	
5.2 BACKLIGHT UNIT	
5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL	
5.4 COLOR DATA INPUT ASSIGNMENT	
5.5 EDID CODE DATA STRUCTURE	
5.6 EDID SIGNAL SPECIFICATION	
6. INTERFACE TIMING	20
6.1 INPUT SIGNAL TIMING SPECIFICATIONS	
6.2 POWER ON/OFF SEQUENCE	
7. OPTICAL CHARACTERISTICS	22
7.1 TEST CONDITIONS	
7.2 OPTICAL SPECIFICATIONS	
8. PRECAUTIONS	26
8.1 ASSEMBLY AND HANDLING PRECAUTIONS	
8.2 SAFETY PRECAUTIONS	
9. PACKING	27
9.1 CARTON	
9.2 PALLET	
10. DEFINITION OF LABELS	28
10.1 CMO MODULE LABEL	
10.2 CMO CARTON LABEL	

**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver 1.0	Nov. 21, '05	All	All	Preliminary Specification was first issued
Ver 1.1	Feb. 08, '06	7	3.1	Modify Power Supply Current to 430 (White) and 560 (Black)
		9	3.2	Modify Power Consumption from 9.42 to 4.7
		18	5.5	Modify EDID Checksum from 3F to 3A
		28	9	Modify Carton label location and Pallet method
		29	10.1	Modify Module Label, cancel customer internal code
		29	10.2	Modify Carton Label, add "GP" mark and "Made in Taiwan"
		30	Drawing	Modify upper bezel, add 2 screw holes
Ver 1.2	Apr. 03, '06	30	Drawing	Modify upper bezel, add 2 screw holes (4 screw holes totally)



1. GENERAL DESCRIPTION

1.1 OVERVIEW

N170C2 - L02 is a 17.0" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1440 x 900 Wide-XGA+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

1.2 FEATURES

- Thin and High Brightness
- WXGA + (1440 x 900 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock
- 1 CCFL

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	367.2 (H) x 229.5 (V) (17.0" diagonal)	mm	(1)
Bezel Opening Area	370.7 (H) x 233.0 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1440 x R.G.B. x 900	pixel	-
Pixel Pitch	0.255 (H) x 0.255 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Glare Type	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	381.7	382.2	382.7	mm	(1)
	Vertical (V)	244.0	244.5	245.0	mm	
	Depth (D)	5.9	6.2	6.5	mm	
Weight		---	670	700	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

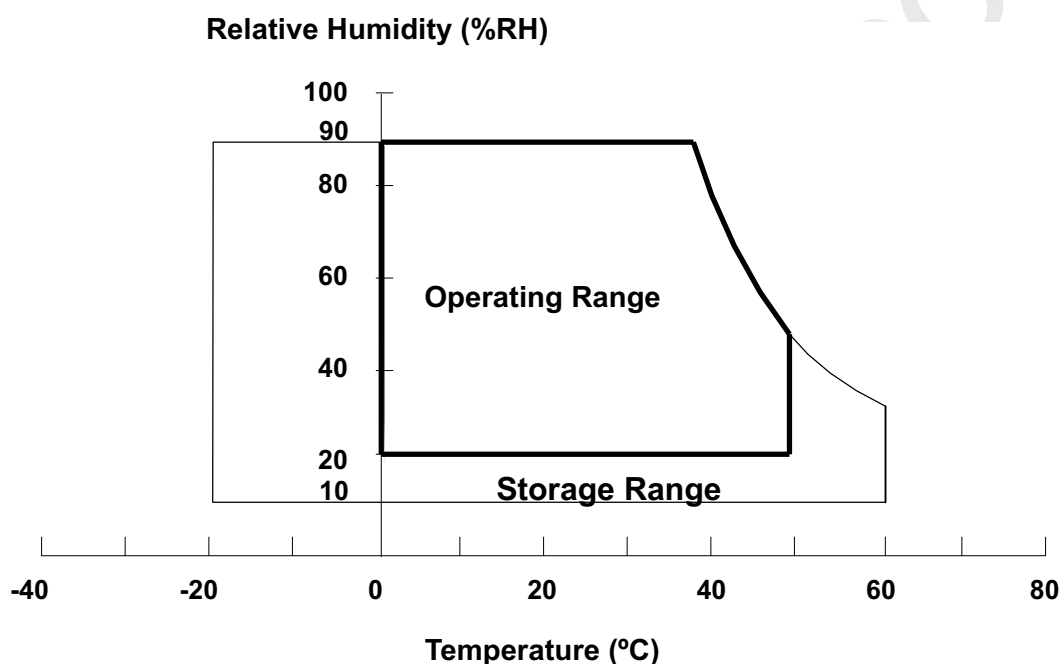
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	200/2	G/ms	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta ≤ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.

Note (2) The temperature of panel display surface area should be 0 °C Min. and 60 °C Max..



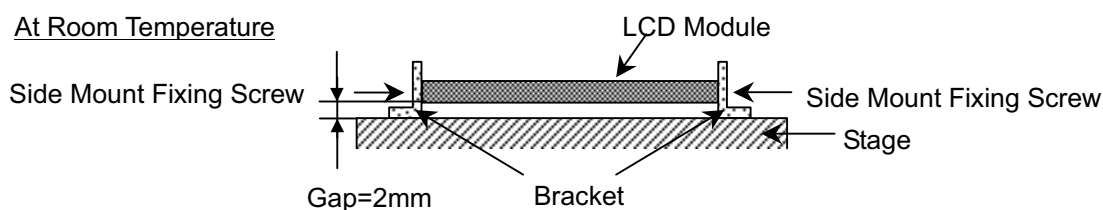
Note (3) 1 time for ± X, ± Y, ± Z. for Condition (200G / 2ms) is half Sine Wave,.

Note (4) 10 ~ 500 Hz, 30 min/cycle, 1 cycles for each X, Y, Z axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:

At Room Temperature



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	$V_{CC}+0.3$	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_L	--	(2.5K)	V_{RMS}	(1), (2), $I_L = 6.0 \text{ mA}$
Lamp Current	I_L	(2.0)	(7.0)	mA_{RMS}	(1), (2)
Lamp Frequency	F_L	(45)	(80)	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

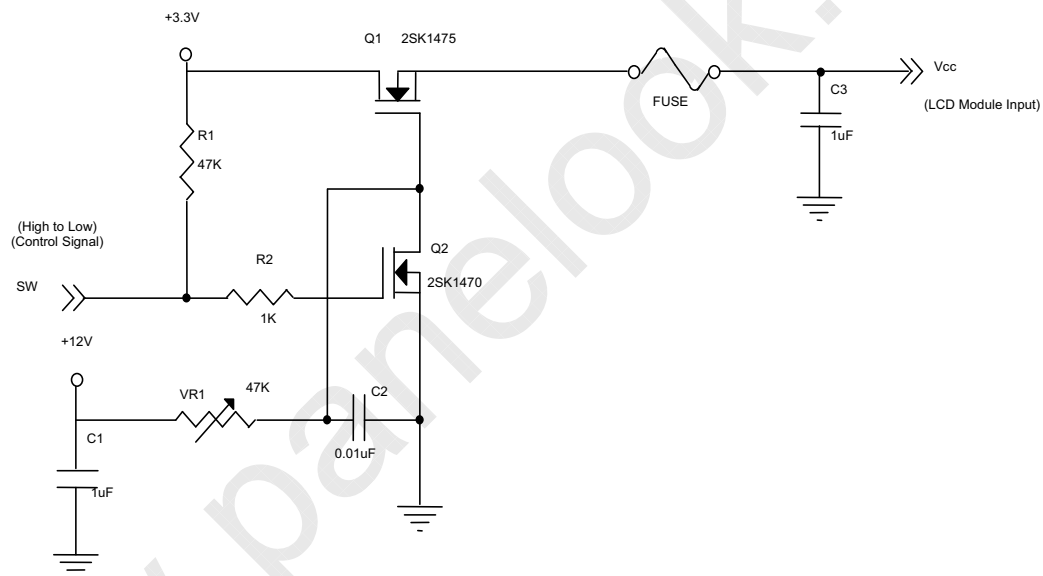
3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

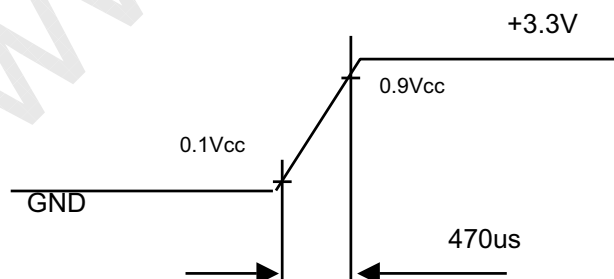
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V _{CC}	3.0	3.3	3.6	V	-
Ripple Voltage	V _{RP}		100		mV	-
Rush Current	I _{RUSH}		1.5		A	(2)
Power Supply Current	White	L _{CC}	(430)	(480)	mA	(3)a
	Black		(560)	(610)	mA	(3)b
Logical Input Voltage	"H" Level	V _{IL}		+100	mV	-
	"L" Level	V _{IH}	-100		mV	-
Terminating Resistor	R _T		100		Ohm	
Power per EBL WG	P _{EBL}	-	TBD	-	W	(4)

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at V_{CC} = 3.3 V, Ta = 25 ± 2 °C, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.



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Model No.: N170C2 - L02

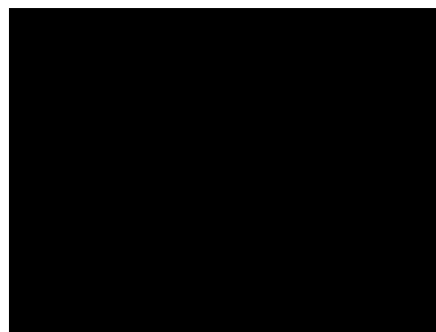
Preliminary

a. White Pattern



Active Area

b. Black Pattern



Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

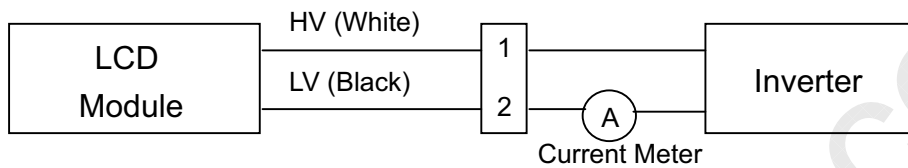
- (a) $V_{cc} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits.
- (d) The inverter used is provided from XXXX(www.XXX.com). CMO doesn't provide the inverter in this product.

3.2 BACKLIGHT UNIT

 $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	(705)	(785)	(855)	V_{RMS}	$I_L = 6.0\text{ mA}$
Lamp Current	I_L	(3.0)	6.0	(7.0)	mA_{RMS}	(1)
Lamp Turn On Voltage	V_s			(1250) ($25\text{ }^{\circ}\text{C}$)	V_{RMS}	(2)
				(1500) ($0\text{ }^{\circ}\text{C}$)	V_{RMS}	(2)
Operating Frequency	F_L	40		80	KHz	(3)
Lamp Life Time	L_{BL}	(12,000)			Hrs	(5)
Power Consumption	P_L		(4.7)		W	(4), $I_L = 6.0\text{ mA}$

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ and $I_L = 6.0\text{ mA}_{RMS}$ until one of the following events occurs:

- When the brightness becomes or lower than 50% of its original value.
- When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.



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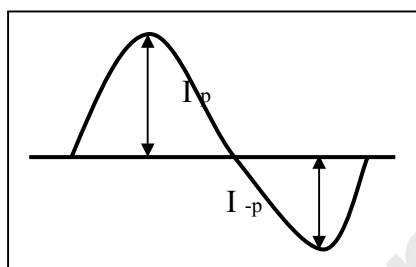
Model No.: N170C2 - L02

Preliminary

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform. (Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- The asymmetry rate of the inverter waveform should be 10% below;
- The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;
- The ideal sine wave form shall be symmetric in positive and negative polarities.



* Asymmetry rate:

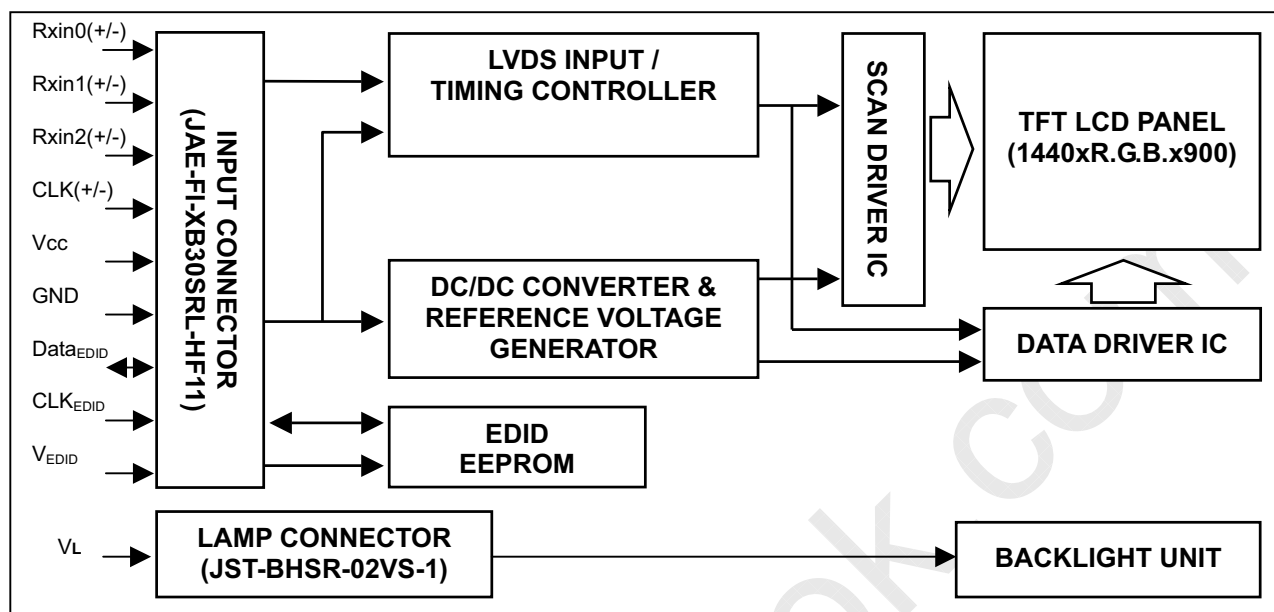
$$|I_p - I_{-p}| / I_{rms} * 100\%$$

* Distortion rate

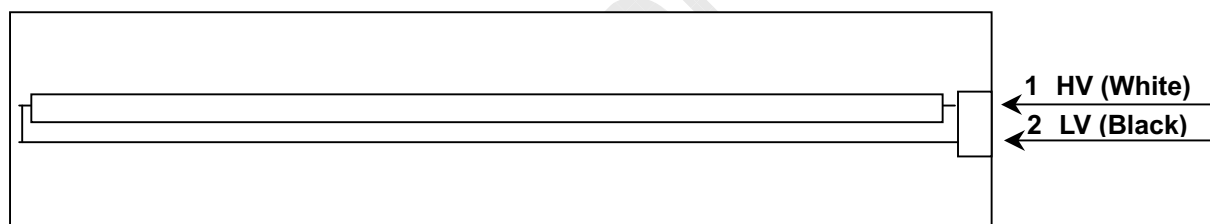
$$I_p \text{ (or } I_{-p}) / I_{rms}$$

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

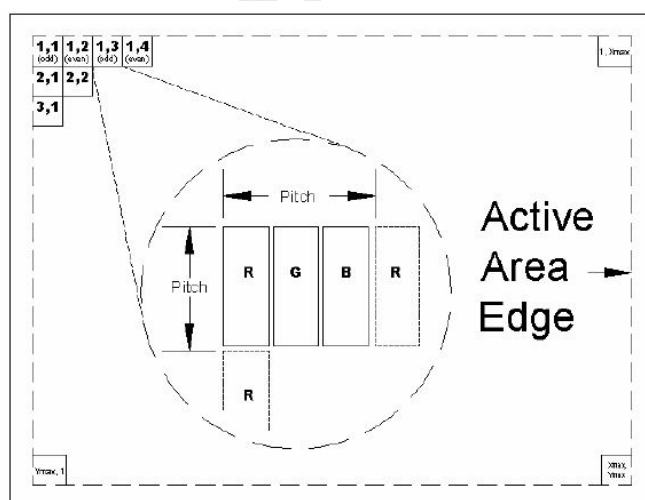
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V _{EDID}	DDC 3.3V Power		
5	NC	Non connection		
6	CLK _{EDID}	DDC Clock		
7	DATA _{EDID}	DDC Data		
8	RX00-	LVDS Differential Data Input (Odd)	Negative	
9	RX00+	LVDS Differential Data Input (Odd)	Positive	
10	Vss	Ground		
11	RX01-	LVDS Differential Data Input (Odd)	Negative	
12	RX01+	LVDS Differential Data Input (Odd)	Positive	
13	Vss	Ground		
14	RX02-	LVDS Differential Data Input (Odd)	Negative	
15	RX02+	LVDS Differential Data Input (Odd)	Positive	
16	Vss	Ground		
17	RXOC-	LVDS Clock Data Input (Odd)	Negative	
18	RXOC+	LVDS Clock Data Input (Odd)	Positive	
19	Vss	Ground		
20	RxE0-	LVDS Differential Data Input (Even)	Negative	
21	RxE0+	LVDS Differential Data Input (Even)	Positive	
22	Vss	Ground		
23	RxE1-	LVDS Differential Data Input (Even)	Negative	
24	RxE1+	LVDS Differential Data Input (Even)	Positive	
25	Vss	Ground		
26	RxE2-	LVDS Differential Data Input (Even)	Negative	
27	RxE2+	LVDS Differential Data Input (Even)	Positive	
28	Vss	Ground		
29	RXEC-	LVDS Clock Data Input (Even)	Negative	
30	RXEC+	LVDS Clock Data Input (Even)	Positive	

Note (1) Connector Part No.: JAE-FI-XB30SRL-HF11 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

Note (3) The first pixel is odd as shown in the following figure.





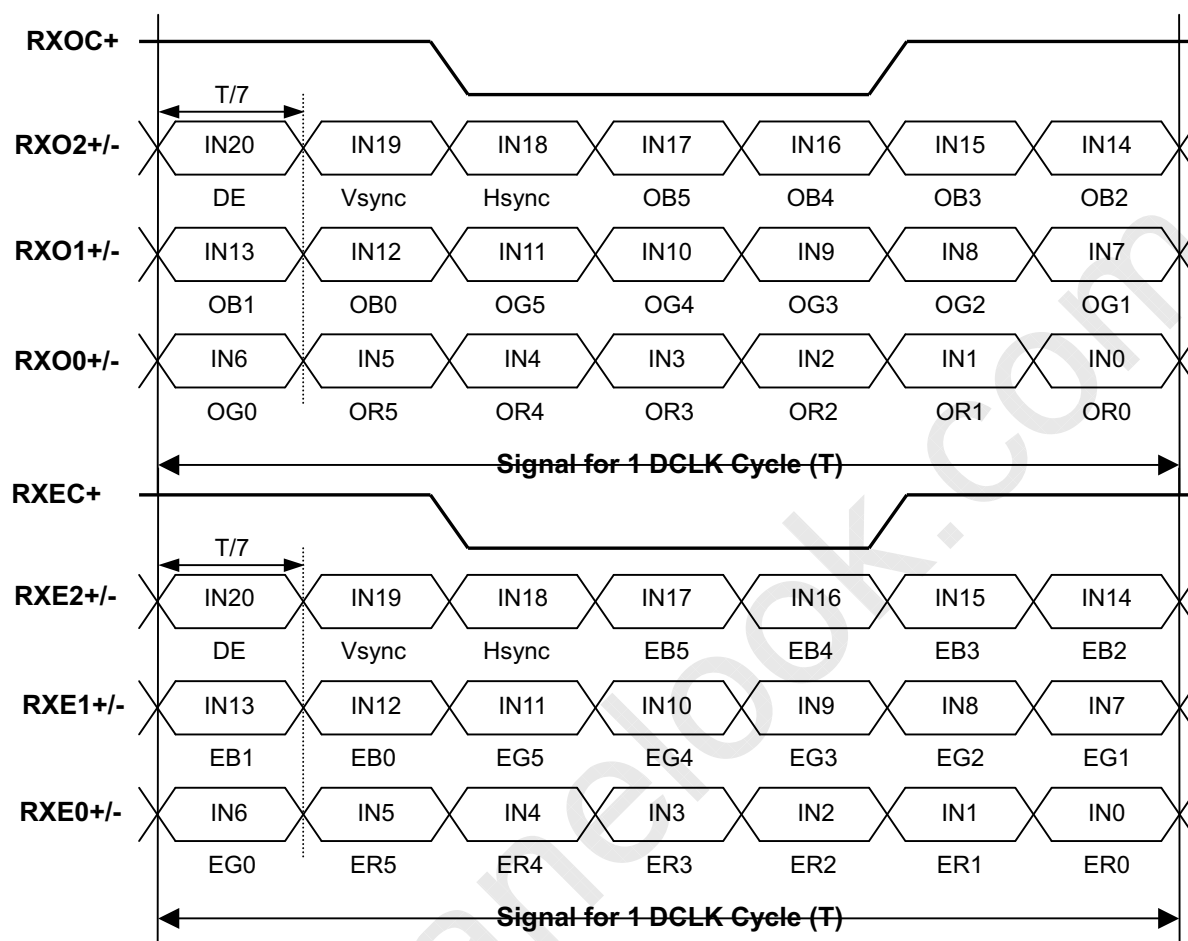
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	White
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD1 standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N170C2-L02)	03	00000011
11	0B	ID product code (hex LSB first; N170C2-L02)	17	00010111
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	0D	00001101
17	11	Year of manufacture (fixed year code)	10	00010000
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	80	10000000
21	15	Active area horizontal 36.72cm	25	00100101
22	16	Active area vertical 22.95cm	17	00010111
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	69	01101001
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	35	00110101
27	1B	Rx=0.571	92	10010010
28	1C	Ry=0.334	55	01010101
29	1D	Gx=0.330	54	01010100
30	1E	Gy=0.567	91	10010001
31	1F	Bx=0.152	27	00100111
32	20	By=0.132	21	00100001
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

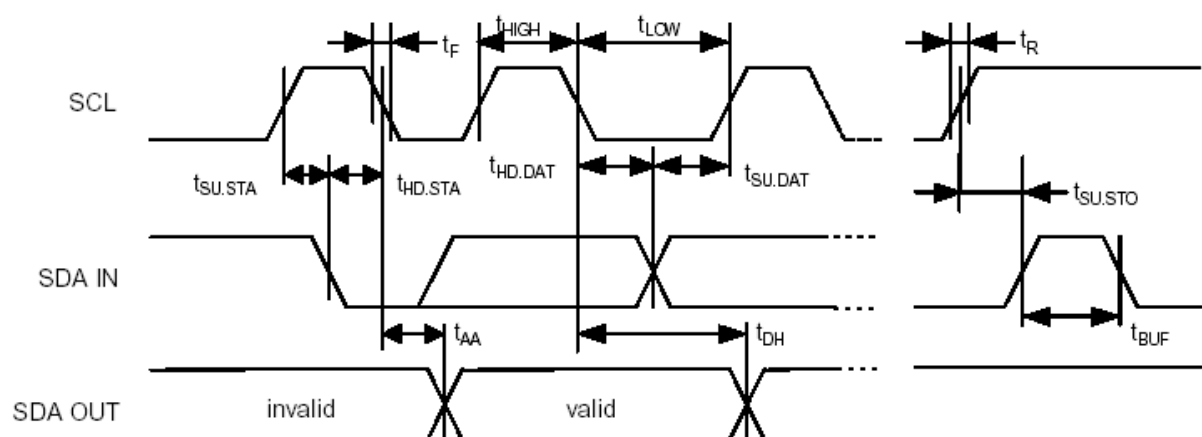
Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("88.75MHz", According to VESA CVT Rev1.1)	AB	10101011
55	37	# 1 Pixel clock (hex LSB first)	22	00100010
56	38	# 1 H active ("1440")	A0	10100000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("1440 : 160")	50	01010000
59	3B	# 1 V active ("900")	84	10000100
60	3C	# 1 V blank ("26")	1A	00011010
61	3D	# 1 V active : V blank ("900 : 26")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 6")	00	00000000
66	42	# 1 H image size ("367 mm")	6F	01101111
67	43	# 1 V image size ("230 mm")	E6	11100110
68	44	# 1 H image size : V image size ("367 : 230")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name "N170C2-L02", ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name ("N")	4E	01001110
78	4E	# 2 2nd character of name ("1")	31	00110001
79	4F	# 2 3rd character of name ("7")	37	00110111
80	50	# 2 4th character of name ("0")	30	00110000
81	51	# 2 5th character of name ("C")	43	01000011
82	52	# 2 6th character of name ("2")	32	00110010
83	53	# 2 7th character of name ("-")	2D	00101101
84	54	# 2 8th character of name ("L")	4C	01001100

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
85	55	# 2 9th character of name ("0")	30	00110000
86	56	# 2 9th character of name ("2")	32	00110010
87	57	# 2 New line character indicates end of ASCII string	0A	00001010
88	58	# 2 Padding with "Blank" character	20	00100000
89	59	# 2 Padding with "Blank" character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor "CMO", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string ("C")	43	01000011
96	60	# 3 2nd character of string ("M")	4D	01001101
97	61	# 3 3rd character of string ("O")	4F	01001111
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name "N170C2-L02", ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name ("N")	4E	01001110
114	72	# 4 2nd character of name ("1")	31	00110001
115	73	# 4 3rd character of name ("7")	37	00110111
116	74	# 4 4th character of name ("0")	30	00110000
117	75	# 4 5th character of name ("C")	43	01000011
118	76	# 4 6th character of name ("2")	32	00110010
119	77	# 4 7th character of name ("-")	2D	00101101
120	78	# 4 8th character of name ("L")	4C	01001100
121	79	# 4 9th character of name ("0")	30	00110000
122	7A	# 4 9th character of name ("2")	32	00110010
123	7B	# 4 New line character indicates end of ASCII string	0A	00001010
124	7C	# 4 Padding with "Blank" character	20	00100000
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	3A	00111010

5.6 EDID SIGNAL SPECIFICATION

(1) EDID Power

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	Read Operation	2.2	—	5.5	V



(2) DC characteristics

		Symbol	Min.	Max.	Unit	Index
SCL, SDA terminal input voltage	High Voltage	VIH	$0.7 \times V_{CC}$	—	V	
	Low Voltage	VIL	—	$0.3 \times V_{CC}$	V	
Hysteresis Voltage		VHYS	$0.05 V_{CC}$	—	V	
Output Voltage		VOL1 VOL2	—	0.4 0.6	V	IOL=3mA, CC=2.5V IOL=6mA, CC=2.5V
Input Leak current (Vin =0.1V~VCC)		ILI	-10 -10	10 50	uA	WP=VSS WP=VCC
Output Leak current		ILO	-10	10	uA	Vout =0.1V~VCC, WP=VSS
Terminal capacity(Input, Output)		Cin, Cout	—	10	pF	VCC=5.0V Ta=25°C, Fclk=1.0MHz
Operating current		ICC Write ICC Read	—	3 1	mA	VCC=5.5V, SCL=400KHz
Stillness current (SDA=SCL=VCC) (WP=VSS,A0,A1,A2=VSS)		ICCS	—	30 100	uA	VCC=3.0V VCC=5.5V



(3) AC characteristics (VCC=2.5~5.5V standard operation mode)

Item	Symbol	VCC=2.5V-5.5V (Standard operation mode)		VCC=4.5V-5.5V (High-speed operation mode)		Unit Index	
		Min.	Max.	Min.	Max.		
Clock frequency	Fclk	—	100	—	400	KHz	
Clock High Time	THIGH	4000	—	900	—	ns	
Clock Low Time	TLOW	4700	—	1300	—	ns	
SDA, SCL falling time	TR	—	1000	—	300	ns	
SDA, SCL rising time	TF	—	300	—	300	ns	
START hold time	THD: STA	4000	—	600	—	ns	
START setup time	TSU: STA	4700	—	600	—	ns	
Data input hold time	THD: Data	0	—	0	—	ns	
Data input setup time	TSU: Data	250	—	100	—	ns	
STOP setup time	TSU: STO	4700	—	600	—	ns	
Output decision time from a clock	TAA	—	3500	100	900	ns	
Bus free time	TBUF	4700	—	1300	—	ns	
Rising time of Min VIH, VIL	TOF	—	250	20	250	ns	CB ≤ 100pF
Spike oppression	TSP	—	50	—	50	ns	
A write-in cycle time	TWR	—	10	—	10	ms	Byte and page mode
The number of times of data rewriting	—	1M	—	1M	—	cycles	VCC=5.0V Ta=25°C,

6. INTERFACE TIMING

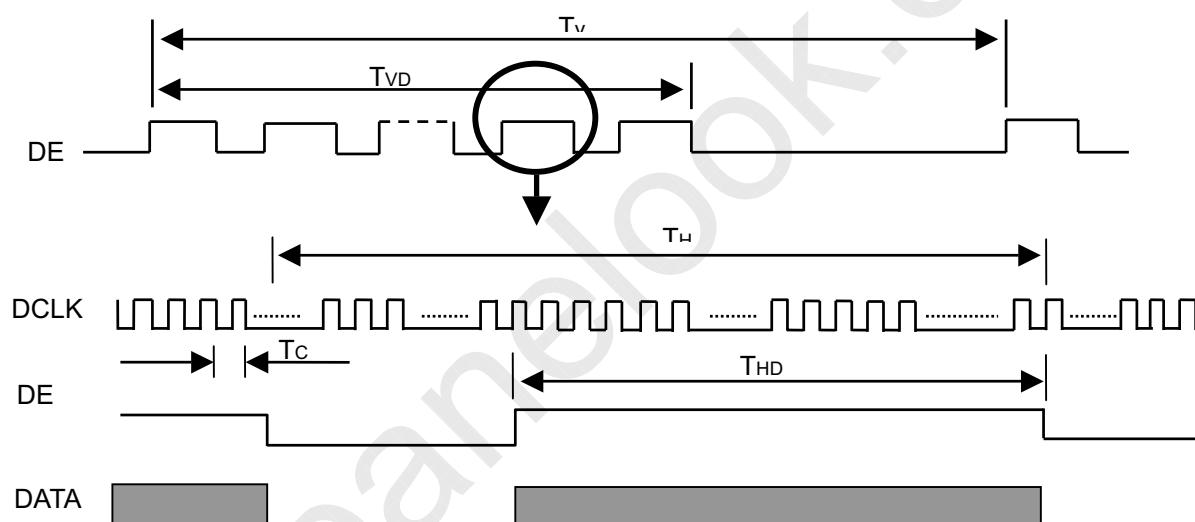
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

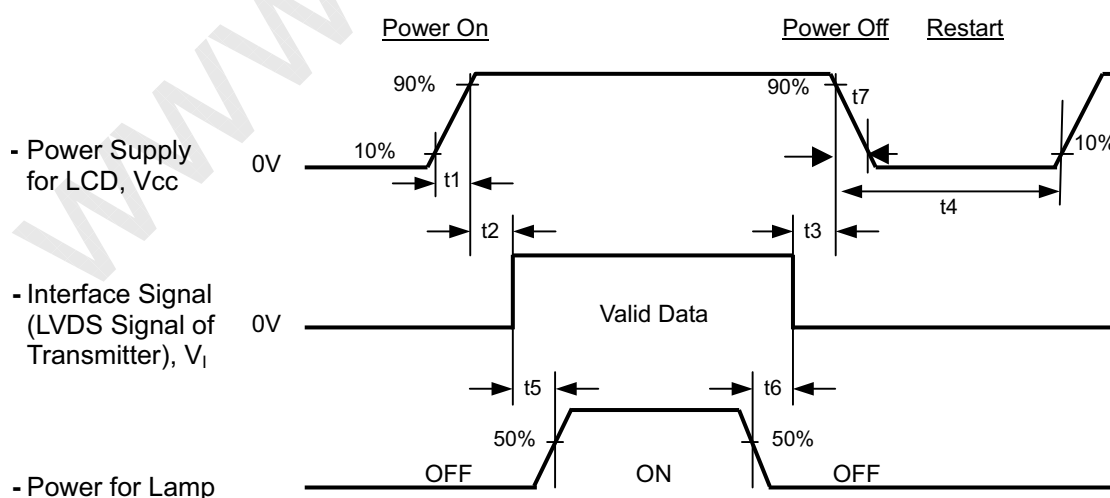
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	25	44.5	60	MHz	-
DE	Vertical Total Time	TV	910	926	1500	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Horizontal Total Time	TH	760	800	880	Tc	-
	Horizontal Active Display Period	THD	720	720	720	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

$$470\mu s < t_1 \leq 10 \text{ ms}$$

$$0 < t_2 \leq 50 \text{ ms}$$

$$0 < t_3 \leq 50 \text{ ms}$$

$$t_4 \geq 500 \text{ ms}$$

$$t_5 \geq 200 \text{ ms}$$

$$t_6 \geq 200 \text{ ms}$$

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow

$$t_7 \geq 5 \text{ msec}$$

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

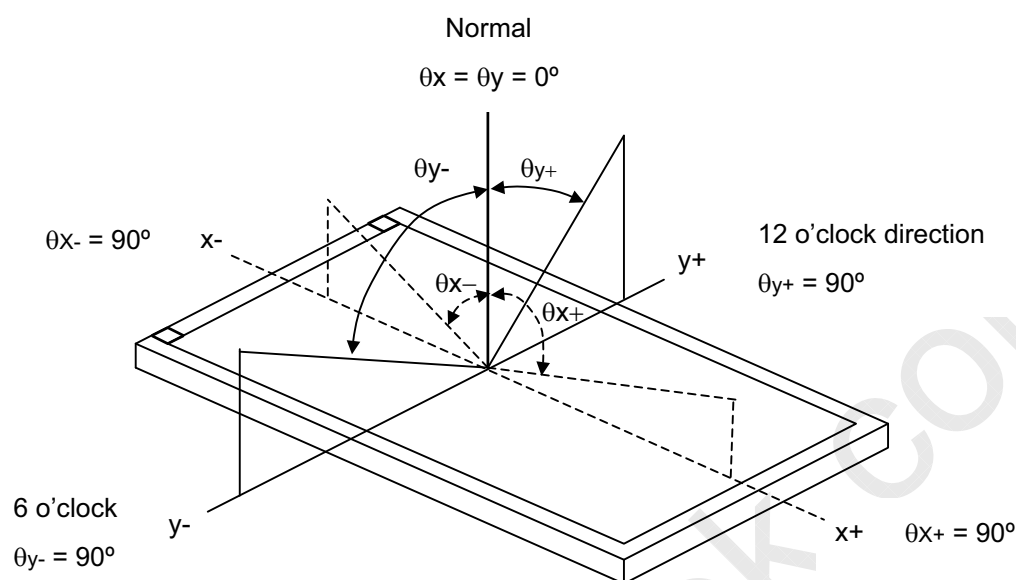
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I _L	(6.0)	mA
Inverter Driving Frequency	F _L	(61)	KHz
Inverter	(Sumida-H05-4915)		

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	R _x	$\theta_x=0^\circ, \theta_Y=0^\circ$ CS-1000T	Typ – 0.03	(0.571)	Typ + 0.03		(1), (5)
		R _y			(0.334)			
	Green	G _x			(0.330)			
		G _y			(0.567)			
	Blue	B _x			(0.152)			
		B _y			(0.132)			
	White	W _x			(0.313)			
		W _y			(0.329)			
Average Luminance of White		L _{AVE}	(170)	(200)	---	cd/m ²	(4), (5)	
Contrast Ratio		CR	(300)	(400)	---	-	(2), (5)	
Response Time		T _R	$\theta_x=0^\circ, \theta_Y=0^\circ$	---	(3)	(8)	ms	(3)
		T _F		---	(7)	(12)	ms	
White Variation		δW	$\theta_x=0^\circ, \theta_Y=0^\circ$	---	(1.25)	(1.40)	-	(5), (6)
Viewing Angle	Horizontal	θ _{x+}	CR ≥ 10 BM-5A	(40)	(45)	---	Deg.	(1), (5)
		θ _{x-}		(40)	(45)	---		
	Vertical	θ _{y+}		(10)	(15)	---		
		θ _{y-}		(30)	(35)	---		

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

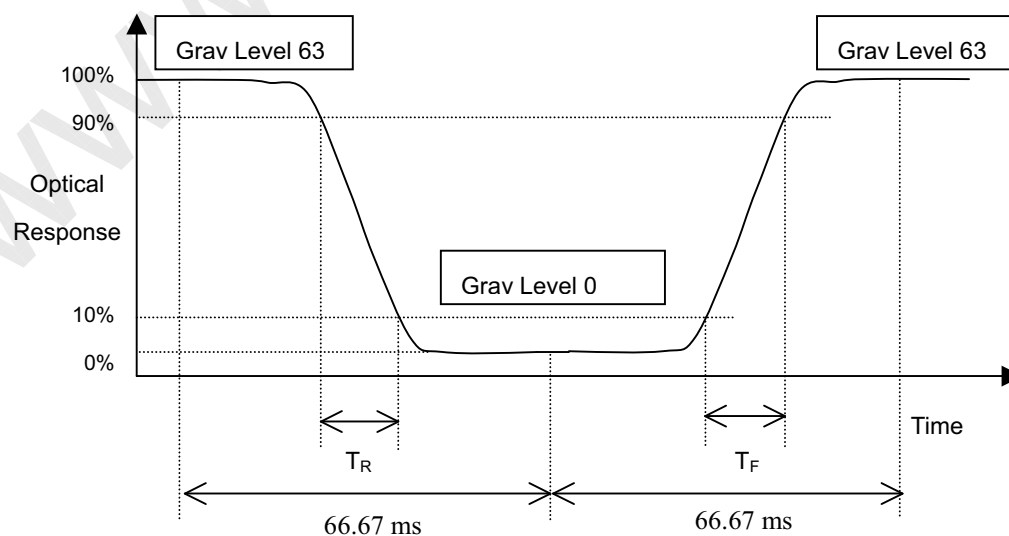
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (1)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

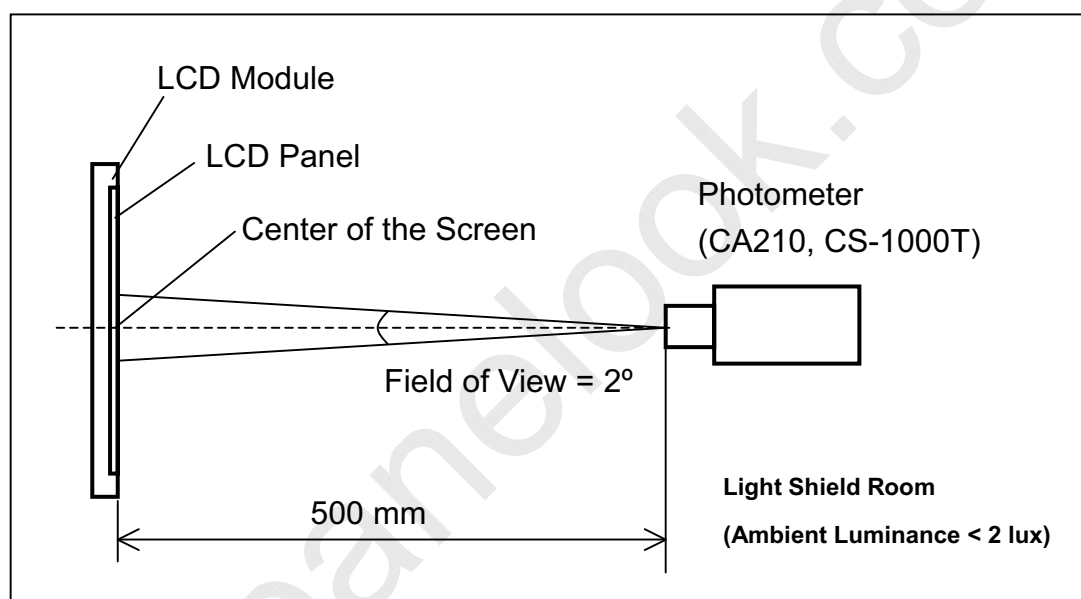
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.





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Issued Date: Apr. 03, 2006

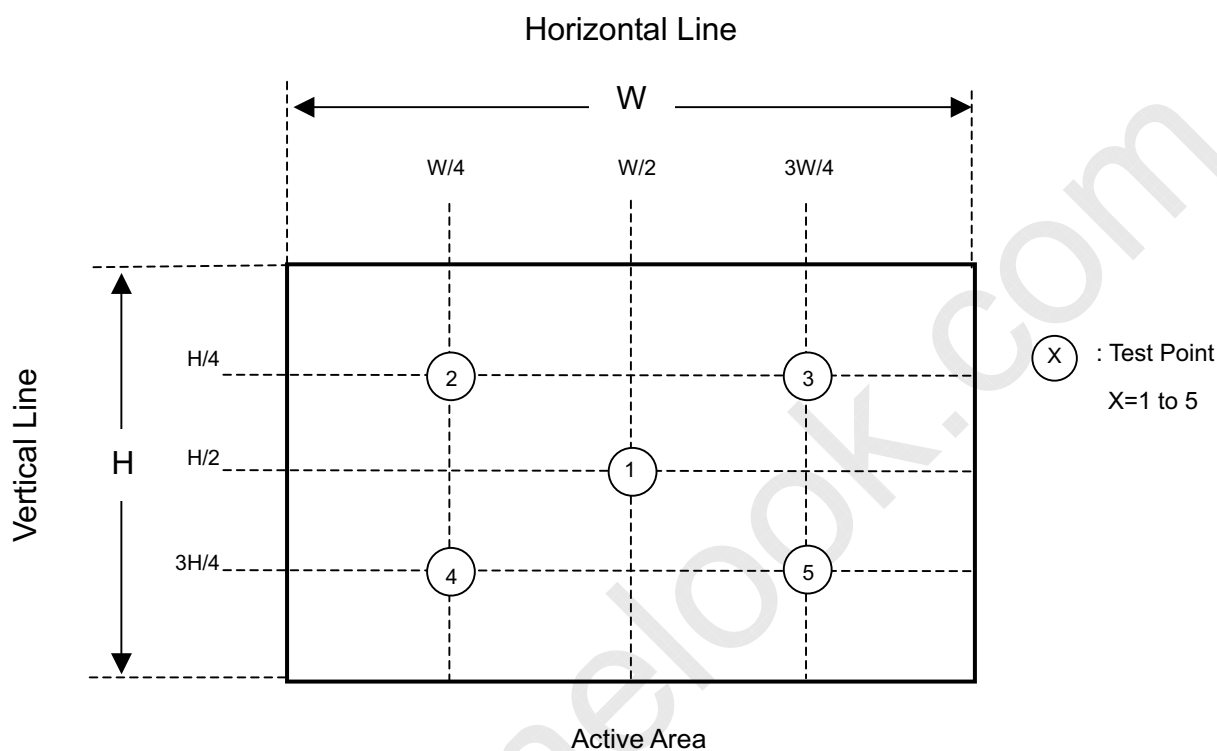
Model No.: N170C2 - L02

Preliminary

Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$$\delta W = \{ \text{Maximum } [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum } [L(1), L(2), L(3), L(4), L(5)] \}$$



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- (4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- (9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (10) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

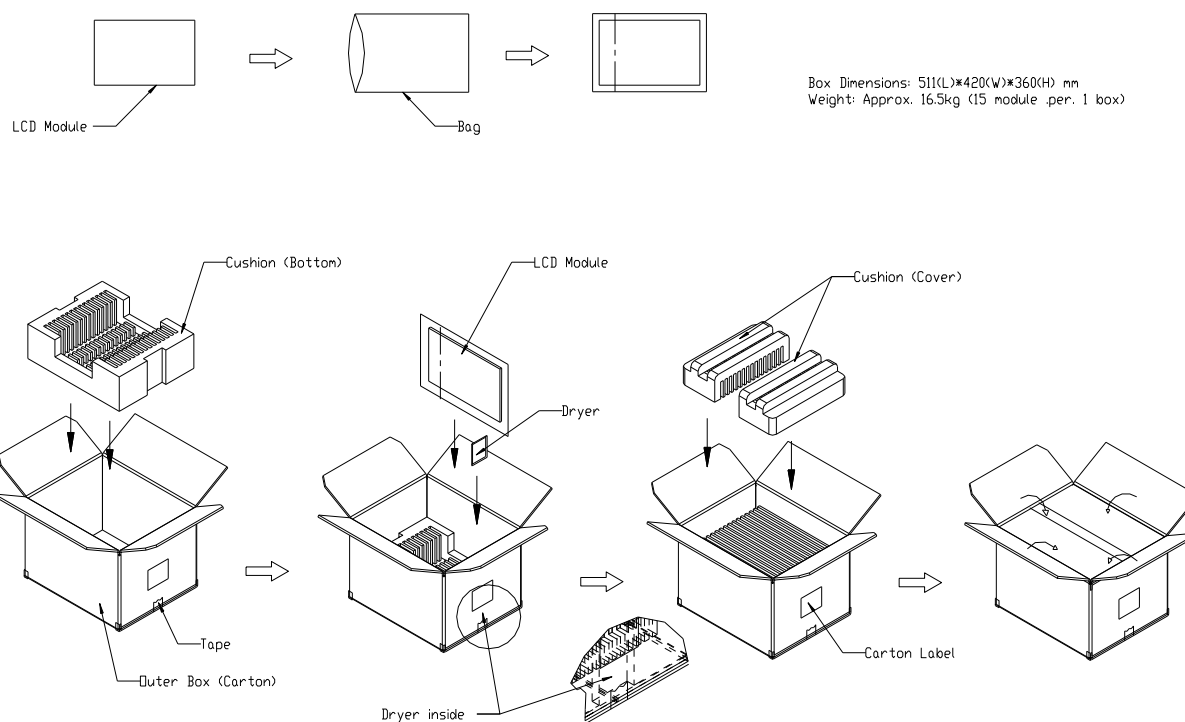
8.2 SAFETY PRECAUTIONS

- (1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

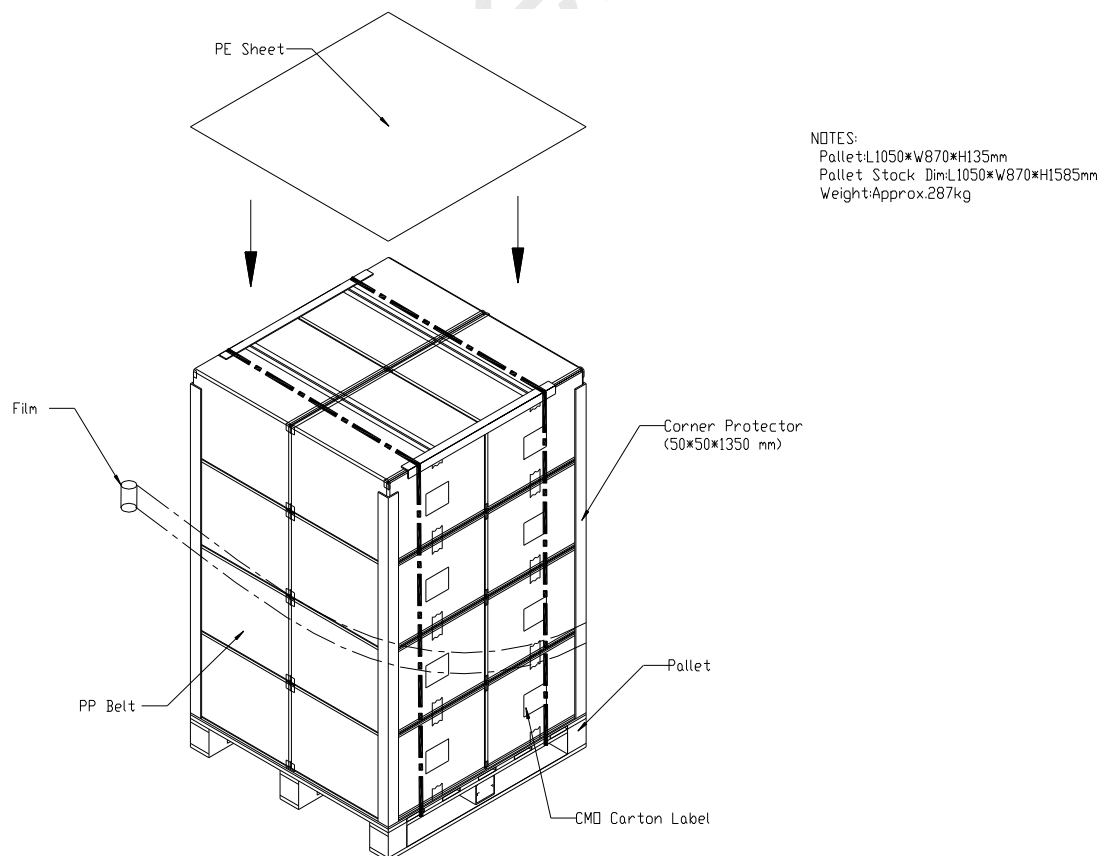


9. PACKING

9.1 CARTON



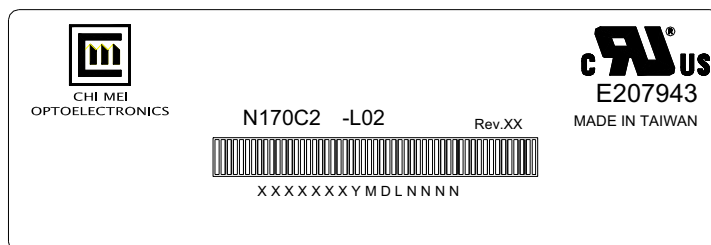
9.2 PALLET



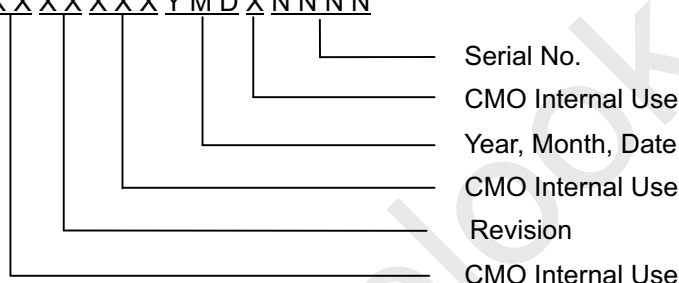
10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



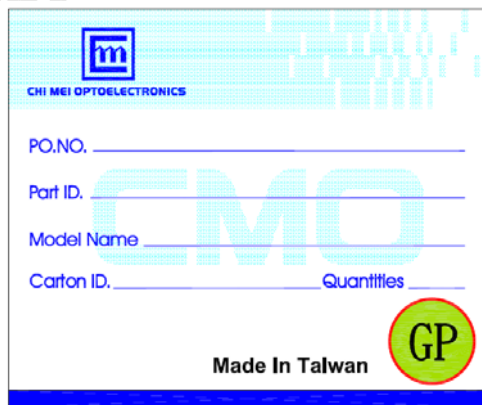
- (a) Model Name: N170C2 - L02
- (b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.
- (c) Serial ID: X X X X X X Y M D X N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2001~2009
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

10.2 CARTON LABEL



CHI MEI OPTOELECTRONICS

PO.NO. _____

Part ID. _____

Model Name _____

Carton ID. _____ Quantities _____

Made In Taiwan

GP



TITLE		ASSY. MODULE, N7022-L01		2D REV. 11	
Approved		Drawing No. N7022-0011		3D REV. 12A	
DAVIS, WANG	Checked	Part No.	TBD		
YALE, LIN	Drawn	Material	TBD		
HSINSHING, CHEN	Design	Date	21-Mar-2005	Scale	1:1
HSINSHING, CHEN	Design	Sheet	1	of	2
Designer		Unltd			
		ALL RIGHTS RESERVED. COPYING FORBIDDEN PATENT/REGISTERED: CHIP			

Sl. No.	Mark	Description	Date	Changed_By	Approved_By	ECN No.	Remark



TITLE	ASSY MODULE N702-1-01							2D REV. I 3D REV. I7
Approved	DAVIS, WANG	Drawing No.	N702A001I					
CHECKED	YULE LIN	Part No.	TBD					
POWER	HONGHAI CHEN	Material	TBD	Sheets	2 / 2	A1		
Designer	HONGHAI CHEN	Date	21-Mar-2005	Scale	I:	Untrim		
ALL RIGHTS RESERVED. COPYING FORBIDDEN						CHI MEI PAPER ENGINEERING CO., LTD.		

Sl. No.	Date	Description	Changed By	Approved By	ECN No.	Remark